A 0.5μm pixel-pitch 200-Megapixel CMOS Image Sensor with Partially Removed Front Deep Trench Isolation for Enhanced Noise Performance and Sensitivity.

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A high-resolution CMOS image sensor is essential in the mobile imaging industry, as a high pixel count enables the capture of finer details and ensures superior image quality under various zoom conditions. Front deep trench isolation (FDTI) technology is a promising solution for achieving this, as it allows submicron-sized pixels to maintain high full-well capacity (FWC) and a high dynamic range (HDR). However, as pixel sizes continue to shrink, integrating FDTI into small pixels presents several challenges. These include reduced FWC due to the smaller photodiode (PD) volume, lower conversion gain (CG) caused by increased metal density, higher temporal random noise (TN) due to the decreased source follower (SF) area, and weaker light focusing due to the limited size of micro-lenses.

One of the key technologies for achieving high performance in small pixels with FDTI is DTI-center-cut (DCC), where a portion of the DTI intersection is partially removed to connect adjacent pixels [1-4]. Adopting the DCC structure in FDTI-based small pixels offers several advantages. First, forming a floating-diffusion (FD) node at the DCC intersection allows adjacent pixels to share the FD junction, reducing FD junction capacitance and thereby increasing CG. Additionally, placing the FD at the DCC intersection simplifies metal wiring, which helps lower metal density and further enhances CG. In particular, in a quad-cell (Q-cell) structure, where four PDs are positioned under a single micro-lens (or Q-cell lens), the DCC structure, which removes part of the DTI at the optical focus point, has the added benefit of reducing light absorption by the polysilicon filling the DTI. In this paper, we present a 200-megapixel (Mp) CMOS image sensor featuring a 0.5μm unit pixel size in the Q-cell FDTI structure. To address the challenges of small-pixel sensors, we introduce the DCC-applied FDTI design along with various technologies that enhance FWC, TN and sensitivity performance.

In the proposed 200Mp CMOS image sensor with the 0.5μm pixel size, a tetra-squared color filter (CF) pattern is applied, where each 4×4 pixel block shares the same color CF, as shown in Fig. 1(a). Fig. 1(b) compares the unit FD configuration in the DCC-applied FDTI structure with that of the conventional FDTI. With DCC, two FD junctions at the intersection of DCCs are connected by a simple metal line, forming a 2×4 structure where eight pixels share the FD region. This approach provides low metal design complexity and low FD junction capacitance while maintaining high CG. In contrast, the conventional FDTI structure without DCC has a higher metal density, which connects the FD junctions of each pixel, increasing the FD capacitance and reducing the CG.

The width of the DCC, denoted by *d* in Fig. 1(c), is a critical design parameter in the DCC-applied FDTI structure. It needs to be wide enough to accommodate the FD junction at the DCC intersection while minimizing light absorption by the polysilicon filling the DTI. However, an excessively broad DCC width lowers the potential barriers between four neighboring PDs, resulting in inter-pixel overflow (IPO). Fig. 2(a) illustrates the potential barrier diagrams for narrow and wide DCC configurations. When the width is sufficiently narrow, the four PDs remain separated by high potential barriers, preserving good signal linearity. As the width increases, however, the potential barrier lowers, causing signal nonlinearity, and a further increase results in white dot noise, as the first readout pixel begins to share photoelectrons with neighboring PDs. Fig. 2(b) shows the

measured white dot noise as a function of the DCC width revealing that white dot noise decreases significantly as the width narrows. Based on the results, we designed the DCC-applied FDTI structure with the sufficient narrow width. The signal linearity with both matched and unmatched chief ray angle (CRA) is shown in Fig. 2(c), indicating that the four PDs are effectively separated by high potential barriers, even with DCC applied.

Fig. 3(a) illustrates the optical structure incorporating various technologies to enhance optical performance : 1) a high-refractive-index Q-cell lens focuses light more intensively; 2) the buried metal of the optical grid is removed to prevent unwanted optical losses caused by the metal; 3) a backside anti-reflection layer (B-ARL) made of high-refractive-index TiO_2, instead of conventional HfO_2, more effectively reduces the reflection of incident light; 4) to further minimize light absorption by the polysilicon in the DTI, the FDTI is filled with SiO_2 instead of 2nd polysilicon layer, as shown in Fig. 3(b). As a result, these technologies improve optical sensitivity by up to 8%. Fig. 3(c) presents the quantum efficiency results, demonstrating improved performance compared to the conventional structure.

To manage noise characteristics in the small pixels with a 0.5μm pixel pitch, three-finger SFs were implemented by connecting three bending-type SFs in parallel. As shown in Fig. 4(a), contact (CNT) walls are also arranged within a 2×4 pixel structure to de-couple the parasitic capacitance between adjacent FDs. When the coupling ratio between neighboring FDs is defined as follows: Inter-pixel coupling ratio [%] = Cap[(FD, JMP, VOUT)$_{center}$-to-FD$_{left,\ right}$]/Cap_FD$_{center}$, the calculated coupling ratios with and without CNT walls are <0.01% and 2.0%, respectively. Fig. 4(b) compares the coupling noise under both conditions, assuming a white spot seed of 1023LSB and an ADC saturation voltage (ADCSAT) with of 1000mV. In addition to the three-finger SFs, the metal/gate stack height was reduced by 40% to decrease input-referred random noise, with an additional increase in CG. Fig. 4(c) illustrates the vertical metal layer structure of the low stack height technology. The noise performance results, compared to those of the previous work [2], are presented in Fig. 4(d).

In summary, we have developed a 200Mp CMOS image sensor with a unit pixel size of 0.5μm based on the Q-cell FDTI structure. By employing the DCC-applied FDTI structure, competitive CG and noise characteristics were achieved. Despite the application of DCC, the linearity of the unit pixel was maintained by designing a sufficiently narrow DCC width to mitigate the effects of IPO. To prevent additional QE loss caused by the narrow DCC size, the polysilicon filling the DTI was partially removed. Additionally, high-refractive-index ARL/micro-lens technology was applied to reduce light reflectance on Si surface and enhance light intensity by minimizing the overlap between the polysilicon in the DTI and the focused light. Fig. 5 shows top chip micrograph and sample image from the developed sensor compared to that of a previous 0.56μm pixel [2]. The key pixel performance results of the developed sensor are summarized in Table 1.

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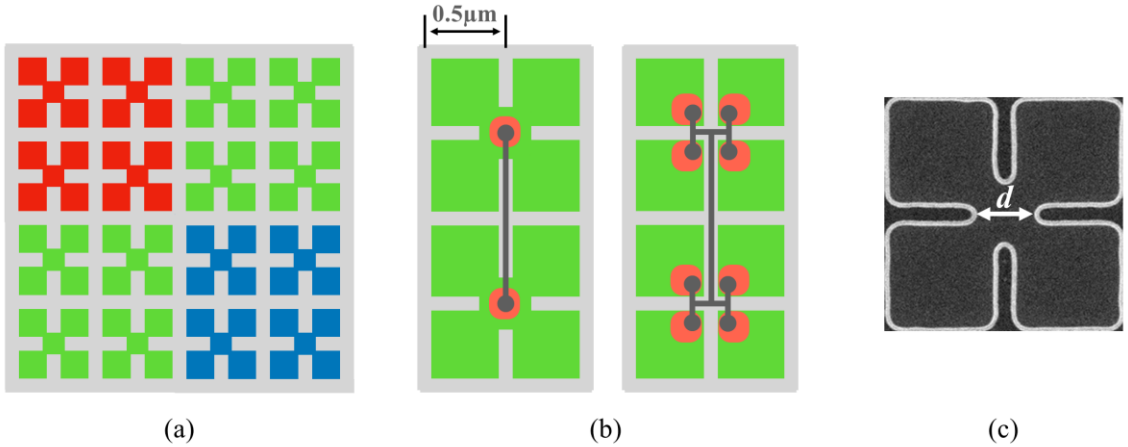

Fig. 1. (a) Schematic of the proposed pixels with the 4×4 CF patterns. (b) Diagrams of 2×4 FD-shared pixel structure with DCC (left) and without DCC (right). (c) Transmission electron microscope (TEM) image of the DCC structure.

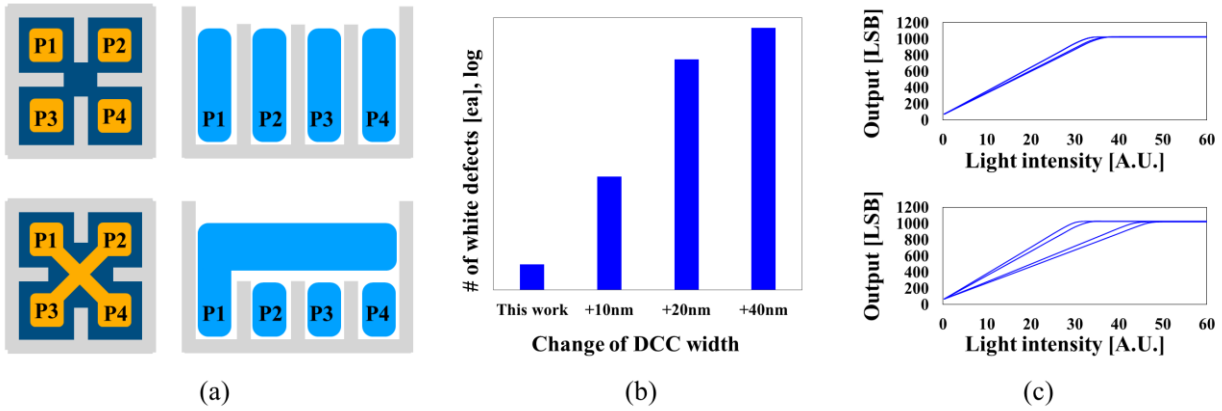

Fig. 2. (a) Conceptual diagrams illustrating the potential barriers between four PDs. Properly separated PDs with the narrow DCC (top) and the PDs exhibiting the significant IPO path due to the wide DCC (bottom). (b) Measured white dot noise results as a function of DCC width. (c) Measured pixel linearity graphs for matched CRA (top) and with unmatched CRA (bottom).

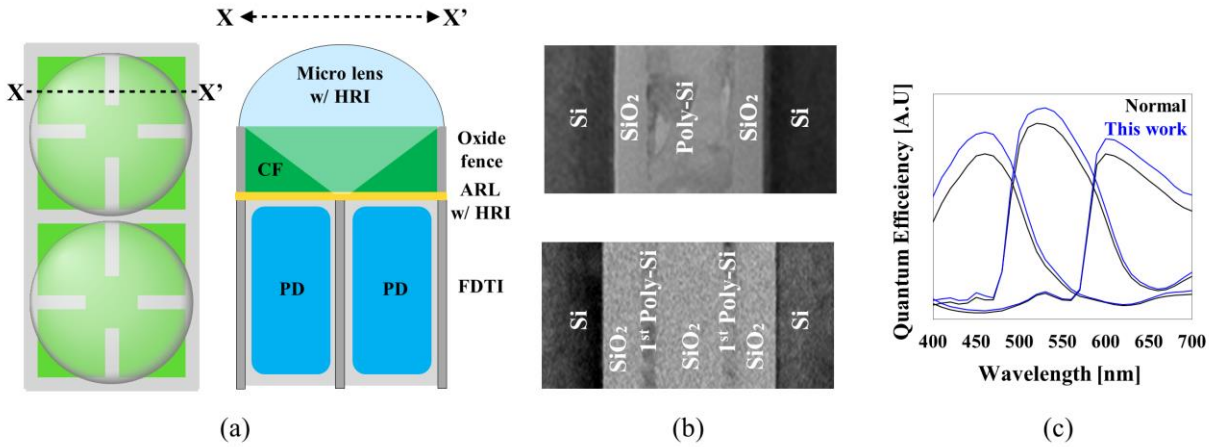

Fig. 3. (a) Schematic illustrations showing the top view of the 2×4 FD-shared pixel structure (left) and the vertical cross-section of the optical structure (right). (b) TEM images of the conventional FDTI filled with 2nd poly-Si (top) and the FDTI filled with SiO_2 (bottom). (c) Measured spectral response results.

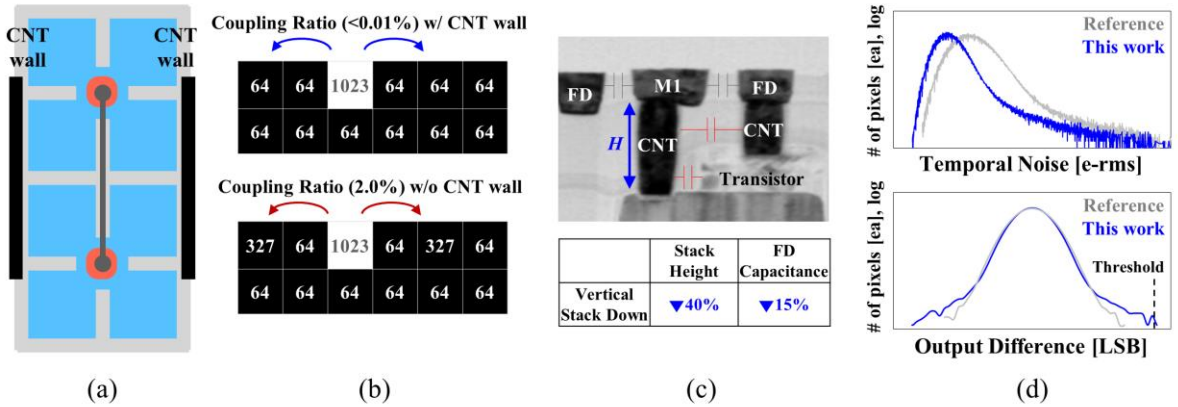

Fig. 4. (a) Schematic illustrating the arrangement of CNT walls in the 2×4 pixel structure. (b) Comparison of coupling noise with CNT walls (top) and without CNT walls (bottom). (c) Vertical cross-sectional TEM image of the metal layer. (d) Measured histograms of temporal random noise (top) and random telegraph signal (RTS) noise (bottom).

Fig. 5. (a) Top chip micrograph. (b) Sample images of the previous work (left) and this work (right).

Items	unit	0.56μm pixel [3]	This work
Photodiode size	μm	0.56 × 0.56	0.5 × 0.5
Full well capacity (full/binning)	e-	4,700 / 75,000	3,700 / 59,000
Temporal noise†	e-	2.3	1.6
Random telegraph signal†	ppm	<1	1
Pixel dynamic range†	dB	90.3	91.3
Sensitivity / Area	e-/lux.sec/μm²	3746	3750

† Pixel Binning Mode

Dynamic Range[dB] = 20 × log(FWC[e-]/TN[e-]

Table 1. Comparison of the overall pixel characteristics between the previous FDTI with DCC-structured small pixels and the pixel structure developed in this work.